Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A method of fabricating contact holes on a semiconductor chip, the semiconductor chip having a substrate comprising:

an array area for locating each memory cell of a dynamic random access memory (DRAM), the array area containing at least a first gate; and

a periphery area for locating a periphery controlling circuit of the DRAM, the periphery area containing at least a second gate;

wherein the first and the second gates comprise a first mask layer on a top surface and a spacer on a sidewall, the method comprising the following steps:

filling a dielectric layer into an inter-gate space;

polishing the dielectric layer to the first mask layer so that a surface of the dielectric layer is approximately coplanar with a surface of the first and second gates;

depositing a second mask layer;

etching the second mask layer to form a bit line opening in the array area, and simultaneously forming a gate opening and a substrate opening in the periphery area;

etching the dielectric layer through the bit line opening

and the substrate opening until a portion of the substrate is exposed so that a bit line contact hole and a substrate contact hole are formed;
filling a metal layer into the bit line contact hole and the substrate contact hole; and
etching the first mask layer through the gate opening.

[c2] 2.The method of claim 1, wherein each of the first and the second gates comprise a conductive layer and a silicide layer.

[c3] 3.The method of claim 2, wherein the conductive layer is composed of dopedpolysilicon.

[c4] 4.The method of claim 2, wherein the substrate contains a gate oxide layer below the first and the second gates.

[c5] 5.The method of claim 4, wherein the gate oxide layer is composed of silicon dioxide (SiO_2).

[c6] 6.The method of claim 1, wherein a glue layer is formed before filling the metal layer into the bit line contact hole and the substrate contacthole.

[c7] 7.The method of claim 6, wherein the glue layer is composed of a titanium nitride (TiN) layer and a titanium (Ti) layer.

[c8] 8.The method of claim 1, wherein the first and second

mask layers are composed of silicon nitride (SiN), silicon carbon (SiC), or silicon oxynitride(SiON).

[c9] 9.The method of claim 1, wherein the dielectric layer is composed of silicon dioxide.

[c10] 10.The method of claim 1, wherein the dielectric layer is composed of borophosphosilicate glass (BPSG).

[c11] 11.The method of claim 1, wherein a thickness of the second mask layer is approximately equal to or greater than a thickness of the first mask layer.

[c12] 12.A method of fabricating contact holes on a semiconductor chip, the semiconductor chip having a substrate comprising:
an array area for locating each memory cell of a DRAM; and
a periphery area for locating a periphery controlling circuit of the DRAM;
wherein the substrate has an oxide layer, a conductive layer, a silicide layer, and a first mask layer thereon, the method comprising the following steps:
removing a portion of the first mask layer, the silicide layer, and the conductive layer to form at least a first gate in the array area and at least a second gate in the periphery array;

forming a spacer on a sidewall of the first and the second gates;

forming a source and a drain at two sides of the first and the second gates;

filling an inter dielectric layer (ILD) into an inter-gate space;

polishing the ILD layer to make the surface of the ILD layer approximately coplanar with the surface of the first mask layer;

depositing a second mask layer, wherein a thickness of the second mask layer is approximately equal to or more than a thickness of the first mask layer;

forming a bit line opening on the second mask layer in the array area, and simultaneously forming a gate opening and a substrate opening on the second mask layer in the periphery area;

removing a portion of the ILD layer through the bit line opening and the substrate opening until a portion of the substrate is exposed, so that a bit line contact hole and a substrate contact hole are formed;

filling a metal layer into the bit line contact hole and the substrate contact hole; and

etching the first mask layer through the gate opening to form a gate contact hole on the first gate.

[c13] 13.The method of claim 12, wherein a glue layer is

formed before filling the metal layerinto the bit line contact hole and the substrate contact hole.

[c14] 14.The method of claim 13, wherein the glue layer is composed of a titanium nitride (TiN) layer and a titanium (Ti) layer.

[c15] 15.The method of claim 12, wherein the oxide layer is composed ofsilicon dioxide.

[c16] 16.The method of claim 12, whereinthe conductive layer is composed doped polysilicon.

[c17] 17.The method of claim 12, wherein the first mask layer is composed of silicon nitride, silicon carbon, or silicon oxynitride.

[c18] 18.The method of claim 12, wherein the second mask layer is composed of silicon nitride, silicon carbon, or silicon oxynitride.

[c19] 19.The method of claim 12, wherein the ILD layer is composed of silicon dioxide.

[c20] 20.The method of claim 12, wherein the ILD layer is composed of borophosphosilicate glass.